High-Efficiency Low-Side N-Channel MOSFET Controller for Switching Regulator

AWT3478Q1

FEATURES

- Wide Input Voltage of 2.97V to 45V
- **6uA** Ultralow Shutdown Current
- 100kHz to 1000kHz Adjustable Clock Frequency
- Current Limit and Thermal Shutdown Protection
- Peak Current Mode Control
- Internal Soft Start
- Internal Gate Driver
- Undervoltage Lockout with Hysteresis
- AEC-Q100 Qualified

APPLICATION

- Distributed Power Systems
- Battery Charger
- Offline Power Supplies
- Telecom Power Supplies
- Automotive Power Systems

DESCRIPTION

The AWT3478Q1 is a versatile Low-Side N-Channel MOSFET controller for switching regulators. It is suitable to drive topologies with a low side N-Channel MOSFET, such as Boost, SEPIC, etc. The operating frequency can be set between 100kHz to 1000kHz by adjusting the resistor value connected to FA/SD pin. Current mode control is adopted to provide high bandwidth, excellent transient response and cycle-by-cycle current limit function.

During output short circuit, the switching frequency is reduced by a factor of 5 to avoid excessive power dissipation until the fault condition is removed. In addition, the AWT3478Q1 has built-in features such as thermal shutdown, over voltage protection, undervoltage lockout, etc. Power saving shut down mode reduces total current to 6uA (Typ.) and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

Typical Application

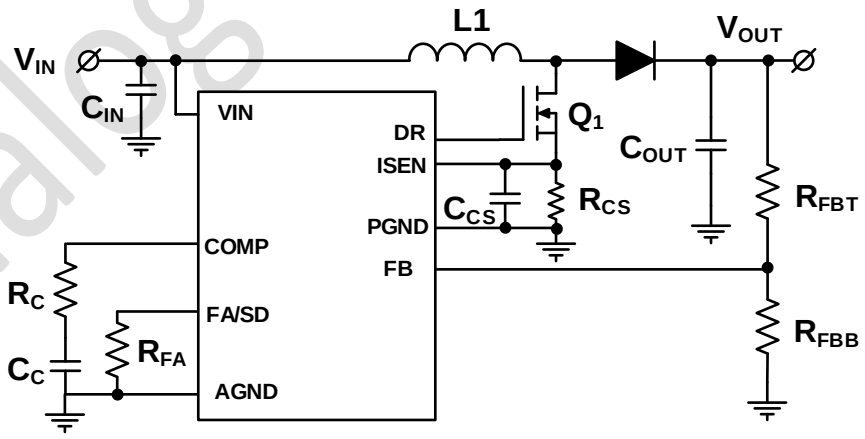

Fig.1 Typical Boost Converter

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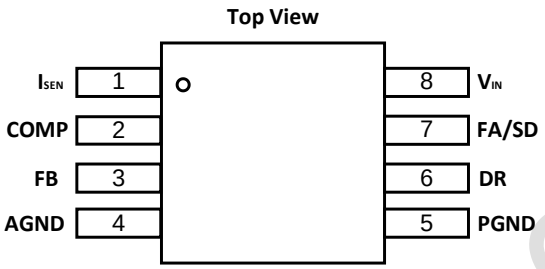
PIN CONFIGURATION

Package	Pin Configuration
MSOP8	

PIN DESCRIPTION

No.	Pin	Type(1)	Description
1	I_{SEN}	O	Current Sense Input
2	COMP	O	Connect a Resistor and a Capacitor for Control Loop Compensation
3	FB	I	Feedback Input
4	AGND	G	Analog Ground
5	PGND	G	Power Ground
6	DR	O	Gate Drive Signal
7	FA/SD	O	Frequency Adjust/Shutdown
8	V_{IN}	P	Power Supply Input

Table 1. AWT3478Q1 Pin Description

(1)P = Power, G = Ground, I = Input, O=Output.

ABSOLUTE MAXIMUM RATINGS

		Min	Max	Units
Input	VIN to GND	-0.3	50	V
	FA/SD to GND	-0.3	5.5	
	FB to GND	-0.3	5.5	
	ISEN to GND	-0.3	1	
Output	DR to GND	-0.3	7.5	V
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	

RECOMMENDED OPERATIONG CONDITIONS

		Min	Max	Units
Boost Regulator	VIN	2.97	45	V
	FA/SD	0	5	
	FB	0	5	
	ISEN	0	0.5	V
	DR	0	7	
T_J	Junction temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±2500	V
	CDM	±750	

ELECTRICAL CHARACTERISTICS

Limits apply over the recommended operating junction temperature range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 5 V. V_{OUT} is converter output voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Operation Input Voltage		2.97		45	V
UVLO	Under Voltage Lockout Thresholds	Rising Threshold		2.7	2.97	V
		Falling Threshold	2.2	2.4		V
I_{SHDN}	Shutdown Supply Current	Vin=5V, $V_{FA/SD}$=5V		6	16	uA
I_{SUPPLY}	Operating Supply Current (Non-Switching) @Sleep Mode	Vin=12V		760	1200	uA
Driver						
$V_{DR(Max)}$	Maximum Drive Voltage	V_{IN} <7.0V		V_{IN}		V
		V_{IN} ≥7.0V		7.0		
T_r(1)	Drive Pin Rising Time	C_{GS} =3.3nF, V_{DR}=0V to 3V		45		ns
T_f(1)	Drive Pin Falling Time	C_{GS} =3.3nF, V_{DR}=3V to 0V		22		ns
Voltage Reference						
V_{FB}	Feedback voltage		1.23	1.26	1.29	V
I_{FB}	Current into FB pin	V_{FB}=1.3V		5		nA
ΔV_{LINE}	Feedback Voltage Line Regulation			0.001	0.01	%/V
ΔV_{LOAD}	Output Voltage Load Regulation	V_{IN}=5V		0.05	0.2	%/A
V_{OVP}	Over Voltage Protection (Respect with Feedback Voltage)			65	145	mV
V_{OVP_HYS}	Over Voltage Protection Hysteresis			30		mV
V_{SENSE}	Current Sense Threshold Voltage		100	155	210	mV
V_{SC}	Short Circuit Current Limit Sense Voltage		290	380	460	mV

Switching Frequency Timing						
f_{SW}	Switching Frequency	R_T=40kΩ	350	400	440	kHz
D_{max}	Maximum Duty Cycle	f_{SW} =400kHz		97		%
T_{ON_MIN}	Min. Turn On Time	f_{SW} =400kHz		270		ns
T_{OFF_MIN}	Min. Turn Off Time	f_{SW} =400kHz		92		ns
T_{SS}	Soft Start	V_{OUT} from 0% to 90%		5		ms
Shutdown						
V_{SD}(2)	Shutdown Rising Threshold			1.15	1.4	V
	Shutdown Falling Threshold		0.65	0.8		V
I_{SD}	Shutdown Pin Current	V_{SD}=5V		0.05		uA
Amplifier						
Gm	Error Amplifier Transconductance	V_{COMP} =1.4V	450	800	1250	uA/V
A_{VOL}	Error Amplifier Voltage Gain		20	55	100	V/V
V_{SL}	Internal Compensation Ramp Voltage	Vin =5V		60		mV
RV_{SL}	V_{SL}/V_{SENSE}			0.4		
I_{EAO}	Error Amplifier Output Current	Source, V_{COMP} =1.4V V_{FB}=0V	55	190	340	uA
		Sink, V_{COMP} =1.4V V_{FB}=1.4V	-175	-110	-60	uA
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit, V_{FB}=0V	2.25	2.55	2.9	V
		Lower Limit, V_{FB}=1.4V	0.5	0.75	1.0	V
Thermal						
T_{SD}	Thermal Shutdown			165		°C
T_{HYS}	Thermal Shutdown Hysteresis			10		°C

Note 1: The rising and falling time are guaranteed by design.

Note 2: The shutdown mode refers to the situation when all modules inside the chip are turned off, which not guarantee that the output will be normal.

FUNCTIONAL DIAGRAM

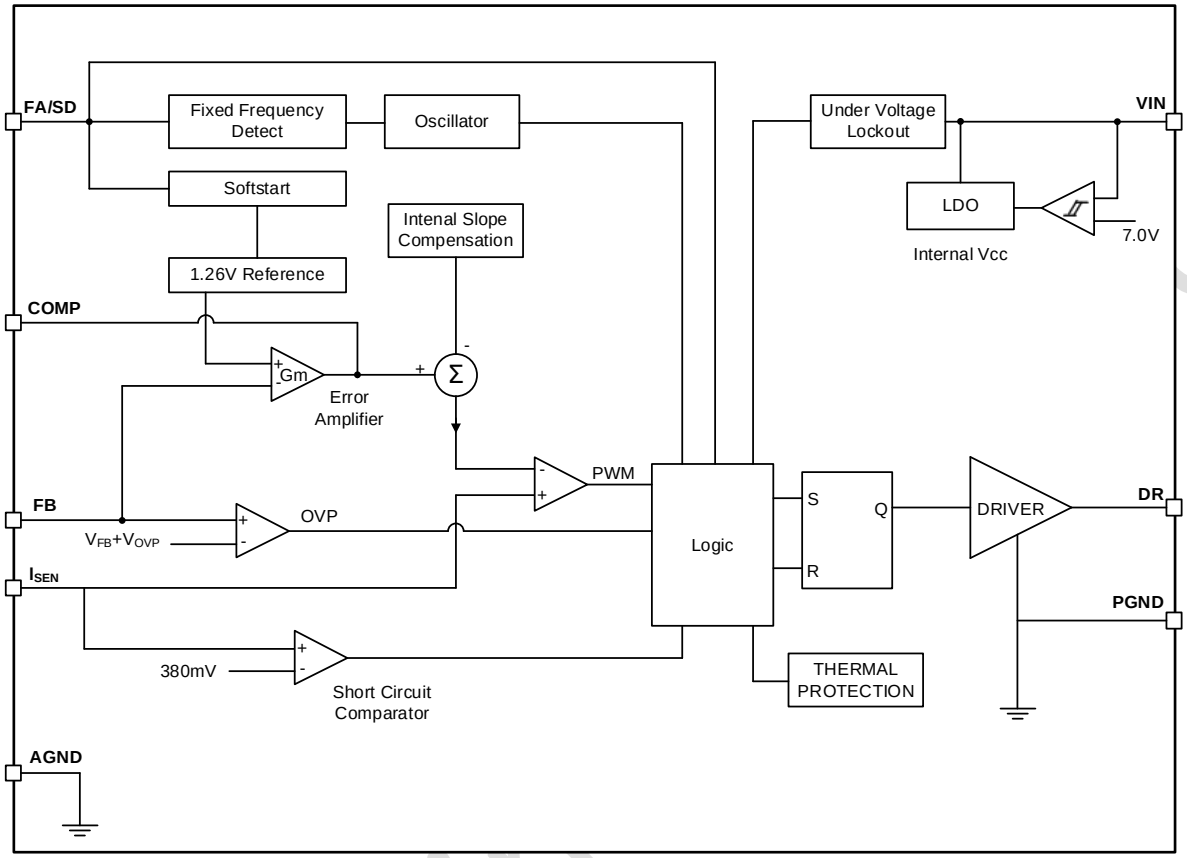


Fig.2 Functional Diagram

TYPICAL CHARACTERISTICS

Unless otherwise specified the following conditions apply: V_{IN} =5V, V_{OUT} =12V, f_{SW} =1000kHz , L=1.8uH, C_{OUT} =188uF, T_A =25°C

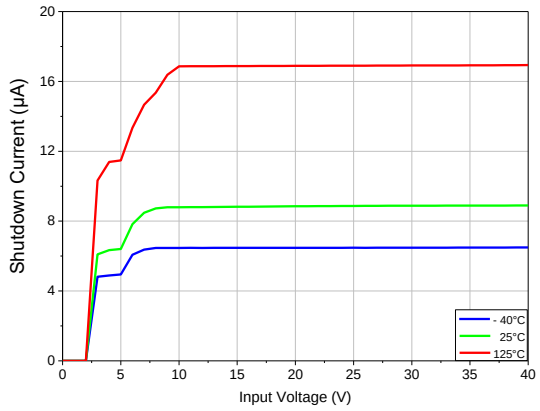


Fig.3 I_{SHDN} VS. Input Voltage

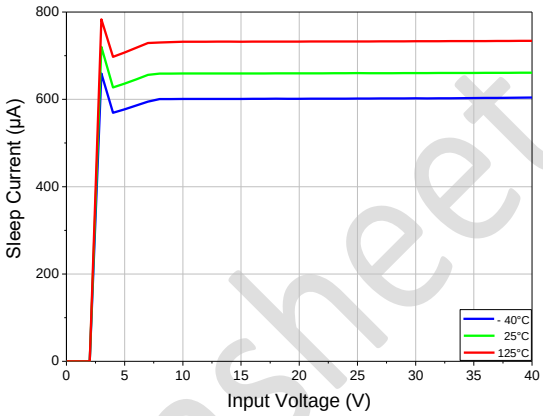


Fig.4 I_{SLEEP} VS. Input Voltage

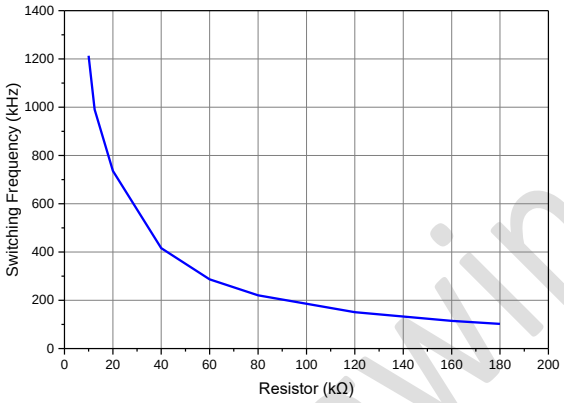


Fig.5. Switching Frequency VS. R_{FA}

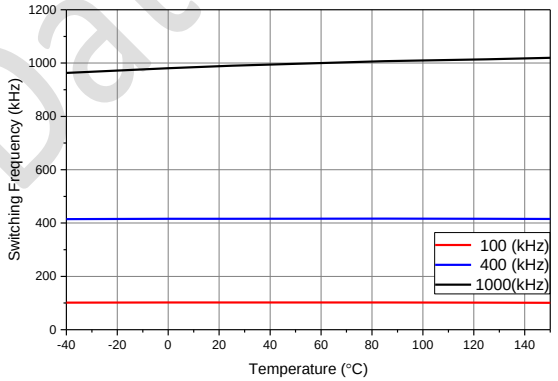


Fig.6 Switching Frequency VS. Temperature

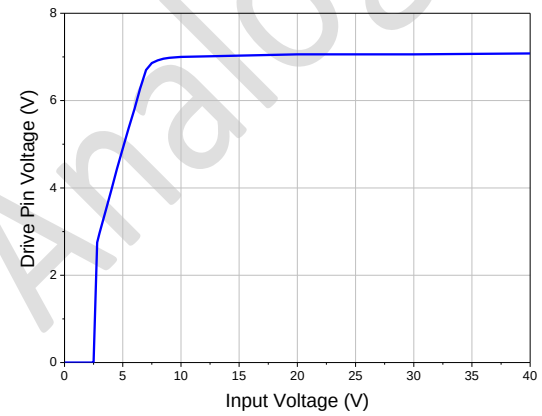


Fig.7 Drive Voltage VS. Input Voltage

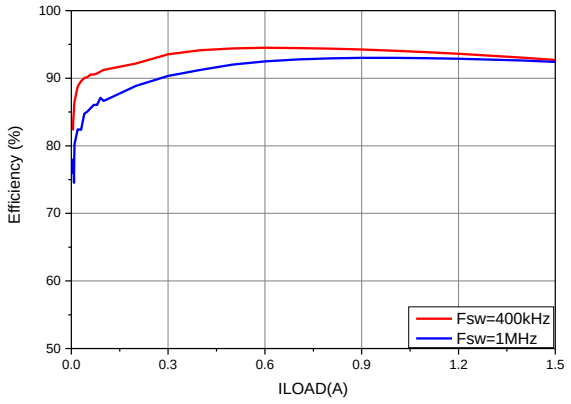


Fig.8 Efficiency VS. Load Current (5V->12V)

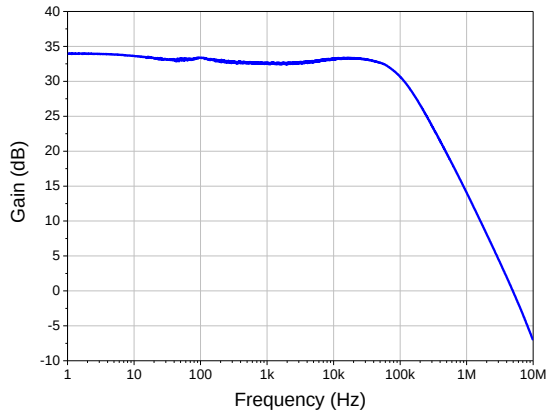


Fig.9 Error Amplifier Gain

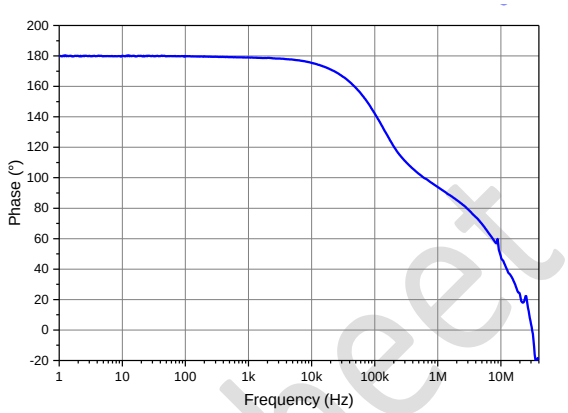


Fig.10 Error Amplifier Phase

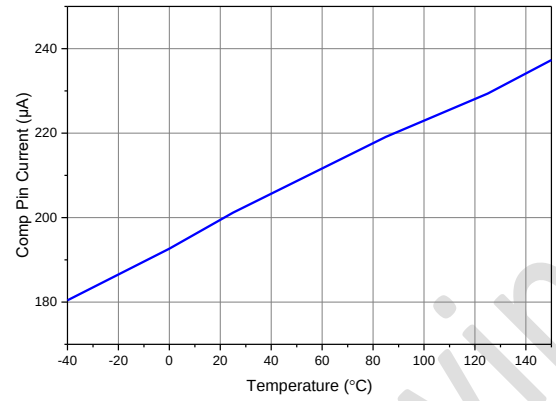


Fig.11 COMP Pin Source Current vs. Temperature

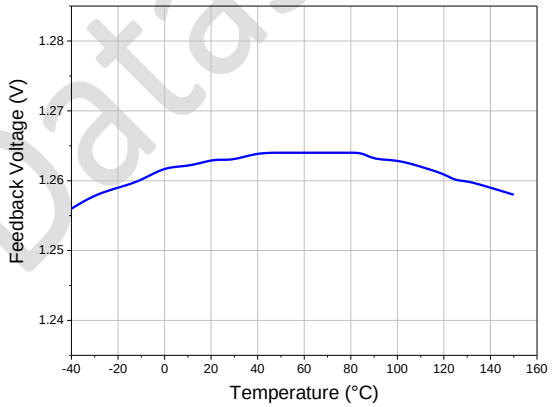


Fig.12 V_{REF} vs. Temperature

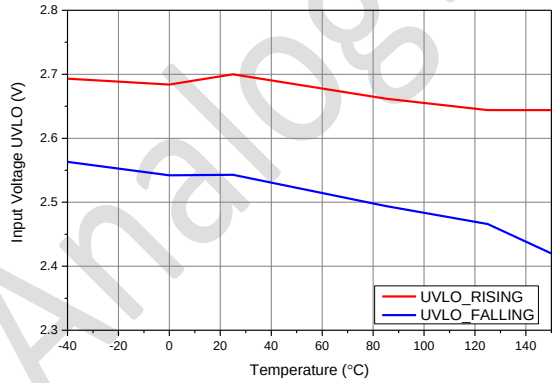


Fig.13 VIN UVLO with Temperature

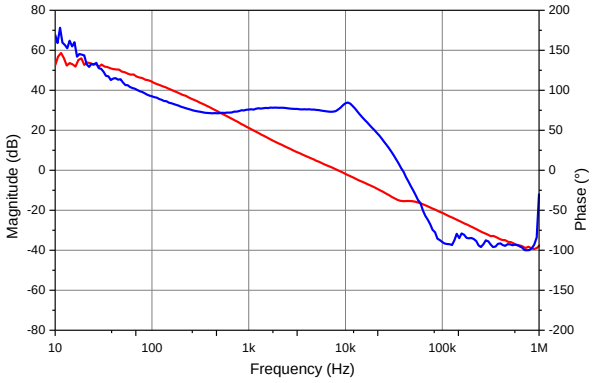


Fig.14 Gain and Phase VS. Frequency (I_{Load}=0.5A)

PRODUCT OVERVIEW

The AWT3478Q1 is a fixed frequency, Pulse Width Modulated (PWM) current mode, versatile Low-Side N-Channel MOSFET controller. It suits for many topologies, such as boost, SEPIC, etc. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the ISEN pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input (Feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

FEATURE DESCRIPTION

Over Voltage Protection

The AWT3478Q1 has over voltage protection (OVP) for preventing the output voltage from rising too high to damage other components. OVP is sensed at the Feedback pin (pin 3).OVP is triggered, when the voltage at the feedback pin rises to $\boldsymbol{V_{FB} + V_{OVP}}$.

OVP will cause the Drive pin (pin 6) to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The AWT3478Q1 will begin switching again when the feedback voltage reaches $\boldsymbol{V_{FB} + (V_{OVP} - V_{OVP(HYS)})}$.

Slope Compensation Ramp

The AWT3478Q1 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. It is also easy to parallel power stages using current mode control since current sharing is automatic. However, current mode control has an inherent instability for duty cycles greater than 50%.

The AWT3478Q1 has some internal slope compensation V_{SL} which is enough for many applications above 50% duty cycle to avoid sub-harmonic oscillation.

Frequency Adjust/Shutdown

The switching frequency of the AWT3478Q1 can be adjusted between 100 kHz and 1 MHz using a single external resistor. This resistor must be connected between FA/SD pin and ground. To determine the value of the resistor required for a desired switching frequency, refer to Typical Characteristics or use following equation:

$$R_T = \frac{18480}{f_{SW}(kHz)} - 6.2(\text{k}\Omega)$$

The FA/SD pin also functions as a shutdown pin. If a high signal (>1.4 V) appears on the FA/SD pin, the AWT3478Q1 stops switching and goes into a low current mode. The total supply current of the IC reduces to less than 6 µA (Typ.) under these conditions. However, the voltage on the FA/SD pin should be always less than the absolute maximum of 5.5 V to avoid any damage to the device.

Short-Circuit Protection

When the voltage across the sense resistor measured on the ISEN pin exceeds 380 mV, short circuit current limit protection gets activated. A comparator inside the AWT3478Q1 reduces the switching frequency by a factor of 5 and maintains this condition until the short is removed. In normal operation the sensed current will trigger the power MOSFET to turn off. During the blanking interval the PWM comparator will not react to an over current so that this additional 380 mV current limit threshold is implemented to protect the device in a short circuit or severe overload condition.

Drive Pin Logic

The internal bias of the AWT3478Q1 comes from the voltage at the VIN, when the input voltage is lower than 7.0V. The internal LDO as shown in the block diagram works when the input voltage is over 7.0V. The frequency of the drive pin signal is determined by the resistance value of the resistor under the pin FA/SD, which can be seen in Frequency Adjust/Shutdown part.

TYPICAL APPLICATIONS

Typical Boost Converter

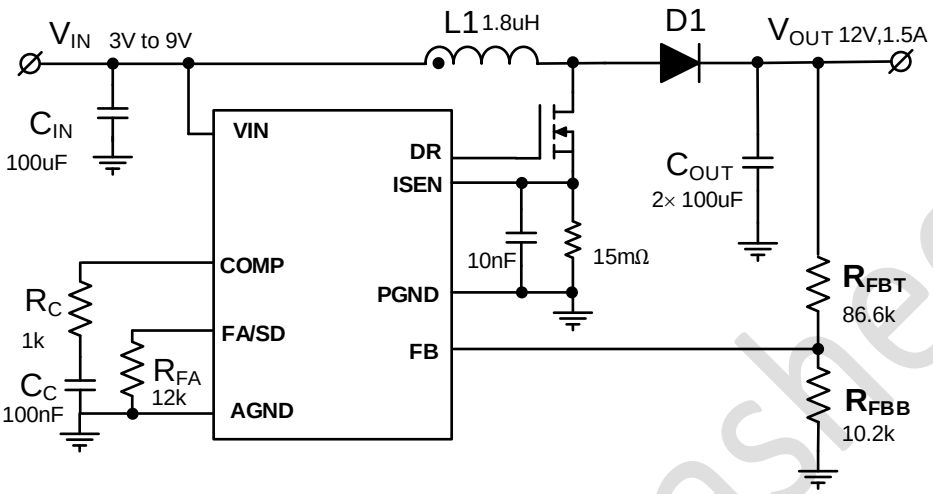


Fig.15 Typical Boost Application Circuit

Setting Output Voltage

The external feedback resistors connected to FB sets the output voltage. The feedback resistor values can be calculated with the below equation.

$$R_{FBB} = \frac{V_{REF} \cdot R_{FBT}}{V_{OUT} - V_{REF}}$$

While R_{FBT}=86.6kΩ, V_{REF}=1.26V, V_{OUT}=12V

Calculate R_{FBB}=10.2kΩ

Setting Switching Frequency

The switching frequency of the AWT3478Q1 can be programmed from 100kHz to 1000kHz by connecting a resistor from RT pin to ground. The typical R_T value can be calculated with the below equation.

$$R_T = \frac{18480}{f_{SW}(kHz)} - 6.2(\text{k}\Omega)$$

The unit of f_{SW} is kHz and the unit of R_T is kΩ.

While we need f_{SW}=1000kHz,

Calculate R_T=12 kΩ.

Inductor Selection

For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 20%-40% of the maximum load current. The inductance value can be calculated with the below equation.

$$L = \frac{V_{IN} \times D}{f_{SW} \times \Delta I_L}$$

While V_{IN}=5V ,V_{OUT}=12V, f_{SW}=1000kHz, D=(12-5)/12≈0.583, ΔI_L=0.4*1.5/(1-0.583)=1.44A

Calculate L=2uH. Considering the size and current selection,1.8uH is selected for typical application.

Power Diode Selection

The selected Diode has a great influence on the system stability. The critical parameters for selecting a Diode are:

1. Peak reverse voltage, V_{RRM}
2. Average forward rectified current, $I_{F(AV)}$
3. Forward voltage, V_F
4. Reverse current, I_R

The peak reverse voltage of the diode should be higher than the maximum voltage of the circuit. The maximum voltage of the circuit appears in the SW node, but the peak voltage depends on several factors, such as PCB layout and selection of components. A good rule for determining the diode value is to select the diode which peak reverse voltage is 20% higher than the output voltage.

The average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current, which can be calculated with the below equation. And it's a good rule to choose 20% to 50% higher than the

$$I_{D(Peak)} = \frac{I_{OUT}}{1 - D} + \Delta I_L$$

The diode should be designed for good thermal conditions, because forward voltage causes power loss. To improve efficiency, a low forward drop Schottky diode is recommended.

AWT3478Q1 can operate in high temperature conditions, which cause the reverse current of the diode to increase. When selecting the diode, make sure the reverse current is low in high temperature situation.

Power MOSFET Selection

The Drive pin of the AWT3478Q1 must be connected to the gate of an external MOSFET. The Drive pin voltage depends on the input voltage. The selected MOSFET has a great influence on the system efficiency. The critical parameters for selecting a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$
2. Minimum threshold voltage, $V_{TH(MIN)}$
3. Continuous Drain Current, I_D
4. On-resistance, R_{DS_ON}
5. Total gate charge, Q_g

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ must be greater than the output voltage.

When selecting MOSFET, the system input voltage state must be considered. Due to the internal LDO, when the input voltage exceeds 7.0V, the high level of the Drive pin stabilizes at 7.0V. A logic level MOSFET can be used. If the input voltage is likely to drop lower, then the $V_{TH(MIN)}$ of the selected MOSFET in any case be guaranteed to be no higher than the minimum input voltage of the system.

The overall power of the system needs to be considered when selecting the MOSFET. The current through the MOSFET can be approximated to the average current through the inductor. The continuous drain current of selected MOSFET should be higher than the input current.

The power losses in the MOSFET can be categorized into conduction losses and switching losses.

$R_{DS(ON)}$ is needed to estimate the conduction losses, P_{COND} can be calculated with the below equation:

$$P_{CONDL} = I_D^2 \times R_{DS\_ON} \times D$$

The temperature effect on the $R_{DS(ON)}$ usually is quite significant. Assume 30% increase at hot.

Especially at high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often the individual MOSFET's datasheet does not give enough information to yield a useful result. The equation below give a rough idea how the switching losses are calculated:

$$P_{SWL} = \frac{I_{LMAX} \times V_{OUT}}{2} \times f_{SW} \times (t_R + t_F)$$

$$t_R = (Q_{GD} + \frac{Q_{GS}}{2}) \times \frac{R_G}{V_{DR} - V_{TH}}$$

Input Capacitor Selection

The input capacitor types can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R,C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. From the below equation, can easily calculate the input voltage ripple. Generally, required the input voltage ripple is less than 10% of the input voltage.

$$\Delta V_{IN} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{IN}}$$

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with equation. Generally, required the output voltage ripple is less than 1% of the output voltage.

$$\Delta V_{OUT} = \frac{I_{OUT} \times (1 - \frac{V_{IN}}{V_{OUT}})}{f_{SW} \times C_{OUT}}$$

Setting Current Sensing Resistor

The switch current is usually used for the peak current mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor R_{SEN} should be less than 70% of the worst-case current limit voltage, 120mV.

$$R_{SEN} = \frac{0.7 \times 0.12}{I_{LPK}}$$

While I_{LPK}=5A, Calculate R_{SEN} =15mΩ.

The value of the current sense voltage varies with the duty cycle of the circuit, and 120mV is only one of the possible detection values for the application conditions. And efficiency should be considered when choosing components, with 85% being a reliable efficiency selection point .

Boost Converter Compensation Design

The AWT3478Q1 uses external components to compensate the regulation loop, for boost topology, an intrinsic right half-plane (RHP) zero is introduced in the regulation feedback loop. the RHP zero introduces a 90-degree phase drop that might cause system instability, furthermore, the location of RPH zero varies with duty cycle and load resistance, which can be determined:

$$f_{RHPZ} = \frac{(1-D)^2 \times R_{LOAD}}{2 \times \pi \times L}$$

where:

f_{RHPZ} is the RHP zero frequency.

R_{LOAD} is the equivalent load resistance.

To stabilized the converter, the crossover frequency is equal to or less than 1/6 of RHP zero frequency and equal to or less than 1/10 of switching frequency. Choose the lower one as crossover frequency.

$$f_{C1} = \frac{f_{RHPZ}}{6}$$

$$f_{C2} = \frac{f_{sw}}{10}$$

By neglecting sampling effect, the regulator loop gain is

$$A_{VL}(f) = \frac{V_{FB}}{V_{OUT}} \times (1-D) \times g_m \times |Z_{COMP}(f)| \times \frac{1}{n \times R_{CS}} \times |Z_{OUT}(f)|$$

where:

A_{VL} is loop gain.

V_{FB} is the feedback regulation voltage.

V_{OUT} is the output voltage.

D is the duty cycle.

gm is the transconductance gain of the error amplifier.

Z_{COMP} is the impedance of the RC network from COMP to GND.

n is the current sense amplifier gain (Typically 1.3).

R_{CS} is the current sense resistor.

Z_{OUT} is the output impedance.

At crossover frequency, the magnitude of the regulator loop gain is 1, it is important to notice that at that frequency, the Z_{OUT} is dominated by output capacitance C_{OUT} and the Z_{COMP} is dominated by the resistor R_{COMP}, then, the loop gain equation can be simplified as

$$|A_{VL}| = \frac{V_{FB}}{V_{OUT}} \times (1 - D) \times g_m \times R_{COMP} \times \frac{1}{n \times R_{CS}} \times \frac{1}{\pi \times f_C \times C_{OUT}}$$

where:

f_c is the crossover frequency.

R_{COMP} is the compensation resistor.

C_{OUT} is the output capacitance.

Solving for R_{COMP} gives

$$R_{COMP} = \frac{V_{OUT} \times 2\pi \times f_C \times C_{OUT} \times n \times R_{CS}}{V_{FB} \times (1 - D) \times g_m}$$

After R_{COMP} is calculated, set the zero formed by resistor and compensation capacitor, C_{COMP}, to 1/4 of the crossover frequency to provide a phase boost for converter stability, the value of compensation capacitor is given by

$$C_{COMP} = \frac{2}{\pi \times R_{COMP} \times f_c}$$

While V_{IN}=5V, V_{OUT}=12V, R_{LOAD}=8Ω, L=1.8uH, Calculate f_{RHPZ} =122.8kHz.

Calculate f_C=20.4kHz.

From above equations, then selected R_{COMP} and C_{COMP} as 1kΩ and 100nF.

APPLICATION WAVEFORMS

Unless otherwise specified the following conditions apply: V_{IN} =5V, V_{OUT} =12V, f_{SW} =1000kHz, L=1.8uH, C_{OUT} =188uF, I_{LOAD_MAX} = 1.5A, T_A =25°C

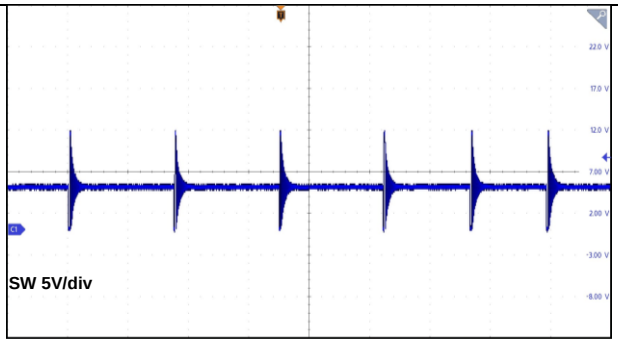


Fig.16 V_{SW} at Io=0A (Steady State)

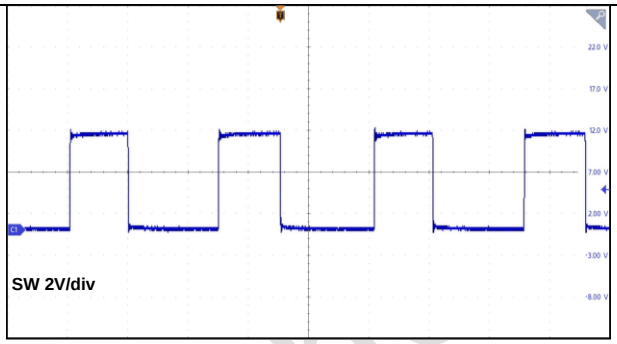


Fig.17 V_{SW} at Io=1A (Steady State)

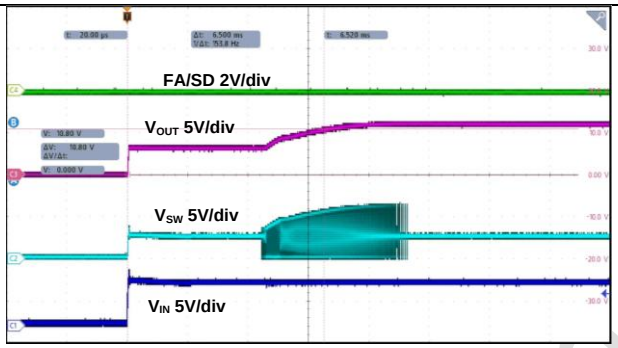


Fig.18 Startup by V_{IN}

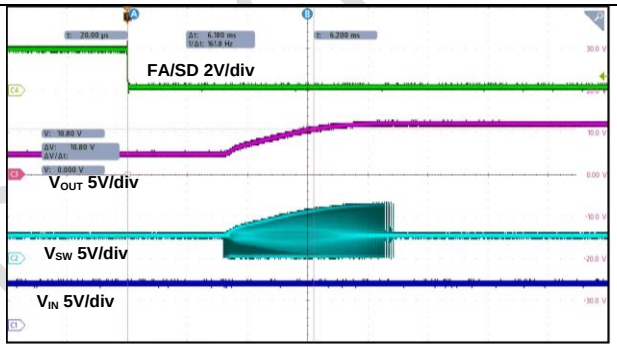


Fig.19 Startup by Disable Shutdown

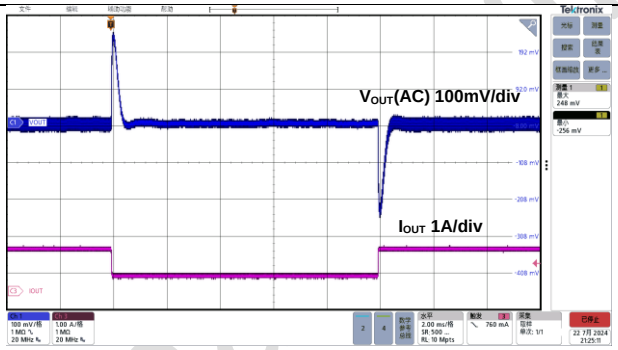


Fig.20 Load Transient @Vin=5V (1A/us)
(I_{Load}: 1.125A->0.375A)

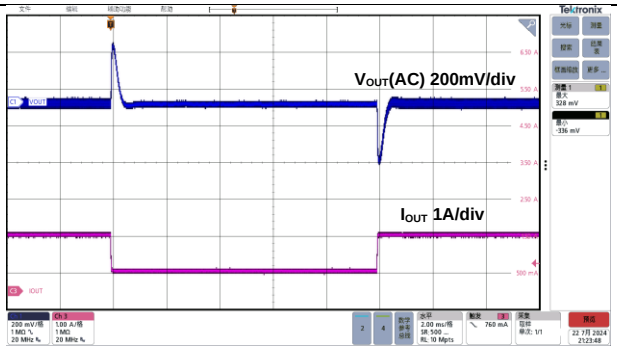


Fig.21 Load Transient @Vin=5V (1A/us)
(I_{Load}: 0. 5A->1.5A)

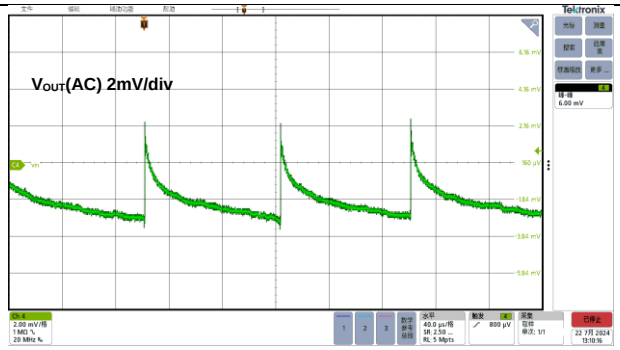


Fig.22 V_{OUT} Ripple at Io=0A (Steady State)

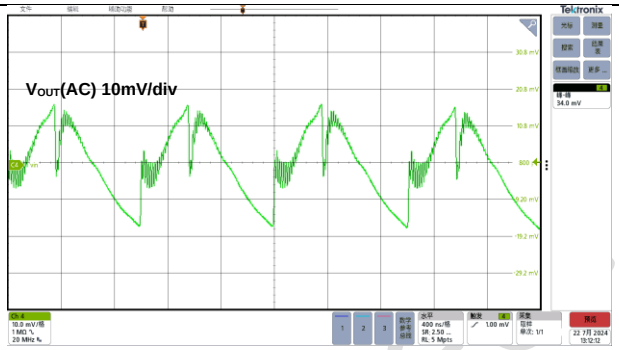


Fig.23 V_{OUT} Ripple at Io=1.5A (Steady State)

Typical SEPIC Converter

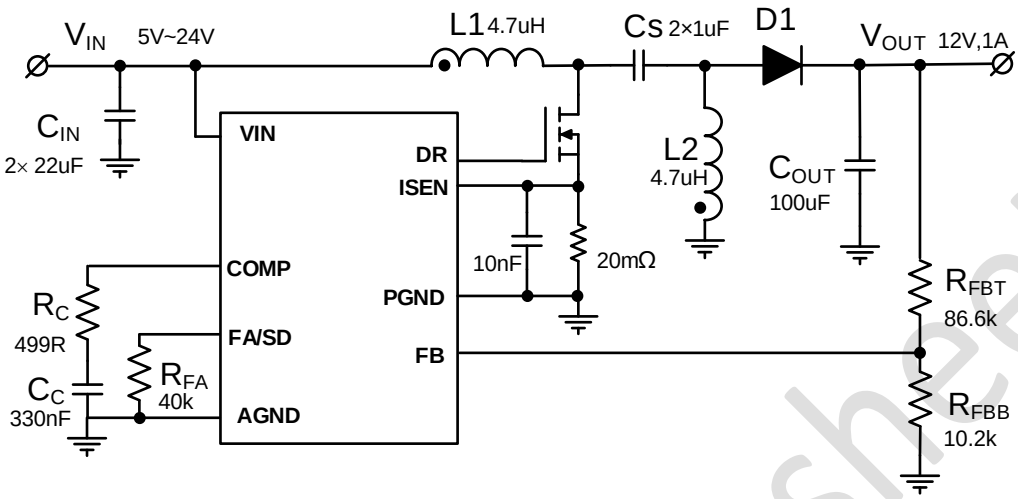


Fig.24 Typical SEPIC Application Circuit

Setting Output Voltage

The external feedback resistors connected to FB sets the output voltage. The feedback resistor values can be calculated with the below equation.

$$R_{FBB} = \frac{V_{REF} \cdot R_{FBT}}{V_{OUT} - V_{REF}}$$

While R_{FBT}=86.6kΩ, V_{REF}=1.26V, V_{OUT}=12V

Calculate R_{FBB}=10.2kΩ

Setting Switching Frequency

The switching frequency of the AWT3478Q1 can be programmed from 100kHz to 1000kHz by connecting a resistor from RT pin to ground. The typical R_T value can be calculated with the below equation.

$$R_T = \frac{18480}{f_{SW}} - 6.2(\text{k}\Omega)$$

The unit of f_{SW} is kHz and the unit of R_T is kΩ.

Setting Current Sensing Resistor

The switch current is usually used for the peak current mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor R_{SEN} should be less than 70% of the worst-case current limit voltage, 160mV.

$$R_{SEN} = \frac{0.7 \times 0.16}{I_{LPK}}$$

While I_{LPK}=5A, Calculate R_{SEN} =20mΩ.

Power Diode Selection

The selected Diode has a great influence on the system stability. The critical parameters for selecting a Diode are:

1. Peak reverse voltage, V_{RRM}
2. Average forward rectified current, $I_{F(AV)}$
3. Forward voltage, V_F
4. Reverse current, I_R

The peak reverse voltage of the diode should be higher than the maximum voltage of the circuit. The maximum voltage of the circuit appears in the SW node, but the peak voltage depends on several factors, such as PCB layout and selection of components. A good rule for determining the diode value is to select the diode which peak reverse voltage is 20% higher than the output voltage.

The average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current, which can be calculated with the below equation.

$$I_{D(Peak)} = \frac{I_{OUT}}{1-D} + \Delta I_L$$

The diode should be designed for good thermal conditions, because forward voltage causes power loss. To improve efficiency, a low forward drop Schottky diode is recommended.

AWT3478Q1 can operate in high temperature conditions, which cause the reverse current of the diode to increase. When selecting the diode, make sure the reverse current is low in high temperature situation.

Power MOSFET Selection

The Drive pin of the AWT3478Q1 must be connected to the gate of an external MOSFET. The Drive pin voltage depends on the input voltage. The selected MOSFET has a great influence on the system efficiency. The critical parameters for selecting a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$
2. Minimum threshold voltage, $V_{TH(MIN)}$
3. Continuous Drain Current, I_D
4. On-resistance, R_{DS_ON}
5. Total gate charge, Q_g

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ must be greater than the output voltage.

When selecting MOSFET, the system input voltage state must be considered. Due to the internal LDO, when the input voltage exceeds 7.0V, the high level of the Drive pin stabilizes at 7.0V. A logic level MOSFET can be used. If the input voltage is likely to drop lower, then the $V_{TH(MIN)}$ of the selected MOSFET in any case be guaranteed to be no higher than the minimum input voltage of the system.

The overall power of the system needs to be considered when selecting the MOSFET. The current through the MOSFET can be approximated to the average current through the inductor. The continuous drain current of selected MOSFET should be higher than the input current.

The power losses in the MOSFET can be categorized into conduction losses and switching losses.

$R_{DS(ON)}$ is needed to estimate the conduction losses, P_{COND} can be calculated with the below equation:

$$P_{CONDL} = I_D^{\,2} \times R_{DS\_ON} \times D$$

The temperature effect on the $R_{DS(ON)}$ usually is quite significant. Assume 30% increase at hot.

Especially at high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often the individual MOSFET's datasheet does not give enough information to yield a useful result. The equation below give a rough idea how the switching losses are calculated:

$$P_{SWL} = \frac{I_{LMAX} \times V_{OUT}}{2} \times f_{SW} \times (t_R + t_F)$$

$$t_R = (Q_{GD} + \frac{Q_{GS}}{2}) \times \frac{R_G}{V_{DR} - V_{TH}}$$

Duty Cycle Consideration

For a SEPIC converter operating in a continuous conduction mode(CCM), the duty cycle is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D}$$

V_D is the forward voltage drop of the diode D1.

Inductor Selection

For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_L = I_{OUT} \times \frac{V_{OUT}}{V_{IN(MIN)}} \times 30\%$$

The inductor value is calculated by:

$$L_1 = L_2 = L = \frac{V_{IN(MIN)}}{\Delta I_L \times f_{SW}} \times D_{MAX}$$

f_{SW} is the switching frequency and D_{MAX} is the duty cycle at the minimum V_{IN} . The peak current in the inductor, to ensure the inductor does not saturate, is given by:

$$I_{L1(PEAK)} = I_{OUT} \times \frac{V_{OUT} + V_D}{V_{IN(MIN)}} \times (1 + \frac{30\%}{2})$$

$$I_{L2(PEAK)} = I_{OUT} \times (1 + \frac{30\%}{2})$$

If using coupled inductor, the value of inductance in the equation above is replaced by 2L due to mutual inductance. The inductor value is calculated by:

$$L1' = L2' = \frac{L}{2} = \frac{V_{IN(MIN)}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX}$$

Input Capacitor Selection

The input capacitor types can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R,C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. From the below equation, can easily calculate the input voltage ripple. Generally, required the input voltage ripple is less than 10% of the input voltage.

$$\Delta V_{IN} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{IN}}$$

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with equation. Generally, required the output voltage ripple is less than 1% of the output voltage.

$$\Delta V_{OUT} = \frac{I_{OUT} \times (1 - \frac{V_{IN}}{V_{OUT}})}{f_{SW} \times C_{OUT}}$$

SEPIC Coupling Capacitor Selection

The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by:

$$I_{CS(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times V_D}{V_{IN(min)}}}$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic capacitors work well for through-hole applications where the size is not limited and they can accommodate the required RMS current rating.

The peak-to-peak ripple voltage on Cs (assuming no ESR):

$$\Delta V_{CS} = \frac{I_{OUT} \times D_{max}}{C_S \times f_{sw}}$$

A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on Cs. Hence, the peak voltage is typically close to the input voltage.

Setting Current Sensing Resistor

The switch current is usually used for the peak current mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor R_{SEN} should be less than 70% of the worst-case current limit voltage, 160mV.

$$R_{SEN} = \frac{0.7 \times 0.16}{I_{LPK}}$$

While I_{LPK}=5A, Calculate R_{SEN} =20mΩ.

The value of the current sense voltage varies with the duty cycle of the circuit, and 160mV is only one of the possible detection values for the application conditions.

SEPIC Converter Compensation Design

The AWT3478Q1 uses external components to compensate the regulation loop, for boost topology, an intrinsic right half-plane (RHP) zero is introduced in the regulation feedback loop. the RHP zero introduces a 90-degree phase drop that might cause system instability, furthermore, the location of RPH zero varies with duty cycle and load resistance, which can be determined:

$$f_{RHPZ} = \frac{(1-D)^2 \times R_{LOAD}}{2 \times \pi \times L}$$

where:

f_{RHPZ} is the RHP zero frequency.

R_{LOAD} is the equivalent load resistance.

To stabilized the converter, the crossover frequency is equal to or less than 1/6 of RHP zero frequency and equal to or less than 1/10 of switching frequency. Choose the lower one as crossover frequency.

$$f_{C1} = \frac{f_{RHPZ}}{6}$$

$$f_{C2} = \frac{f_{sw}}{10}$$

By neglecting sampling effect, the regulator loop gain is

$$A_{VL}(f) = \frac{V_{FB}}{V_{OUT}} \times (1-D) \times g_m \times |Z_{COMP}(f)| \times \frac{1}{n \times R_{CS}} \times |Z_{OUT}(f)|$$

where:

A_{VL} is loop gain.

V_{FB} is the feedback regulation voltage.

V_{OUT} is the output voltage.

D is the duty cycle.

gm is the transconductance gain of the error amplifier.

Z_{COMP} is the impedance of the RC network from COMP to GND.

n is the current sense amplifier gain (Typically 1.3).

R_{CS} is the current sense resistor.

Z_{OUT} is the output impedance.

At crossover frequency, the magnitude of the regulator loop gain is 1, it is important to notice that at that frequency, the Z_{OUT} is dominated by output capacitance C_{OUT} and the Z_{COMP} is dominated by the resistor R_{COMP}, then, the loop gain equation can be simplified as

$$|A_{VL}| = \frac{V_{FB}}{V_{OUT}} \times (1 - D) \times g_m \times R_{COMP} \times \frac{1}{n \times R_{CS}} \times \frac{1}{\pi \times f_C \times C_{OUT}}$$

where:

f_c is the crossover frequency.

R_{COMP} is the compensation resistor.

C_{OUT} is the output capacitance.

Solving for R_{COMP} gives

$$R_{COMP} = \frac{V_{OUT} \times 2\pi \times f_C \times C_{OUT} \times n \times R_{CS}}{V_{FB} \times (1 - D) \times g_m}$$

After R_{COMP} is calculated, set the zero formed by resistor and compensation capacitor, C_{COMP}, to 1/4 of the crossover frequency to provide a phase boost for converter stability, the value of compensation capacitor is given by

$$C_{COMP} = \frac{2}{\pi \times R_{COMP} \times f_c}$$

While V_{IN}=5V, V_{OUT}=12V, R_{LOAD}=8Ω, L=1.8uH, Calculate f_{RHPZ} =122.8kHz.

$$f_C = \frac{f_{RHPZ}}{6}$$

Calculate f_C=20.4kHz.

From above equations, then selected R_{COMP} and C_{COMP} as 1kΩ and 100nF.

PCB LAYOUT GUIDELINES

PCB layout is critical for stable operation of switching regulator AWT3478Q1, especially for thermal design and EMI design. A four-layer layout is strongly recommended to achieve better thermal performance and EMI performance. For best results, please follow the guidelines below.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible.

2. Place the ground of the current sense resistor as close to the ground of output capacitor as possible.

3. Make sure top switching loop with power have lowest impendence of grounding.

4. Use a large ground plane to connect to GND directly. And add vias near GND.

5. Output inductor should be placed close to the SW pin to minimize the SW area.

6. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.

7. The SENSE and DR terminal is sensitive to noise so the capacitor and resistor of sense filter and the DR resistor should be located as far as possible to the noise source such as the SW area.

8. Keep the connection of the input capacitor and VIN as short and wide as possible.

9. When the power of the output is over than 50W, add vias in the SW area to make sure the thermal performance of MOSFETs. In this situation, the performance of EMI won't be guaranteed.

From Fig.25 to Fig.28, there are some layout examples for reference.

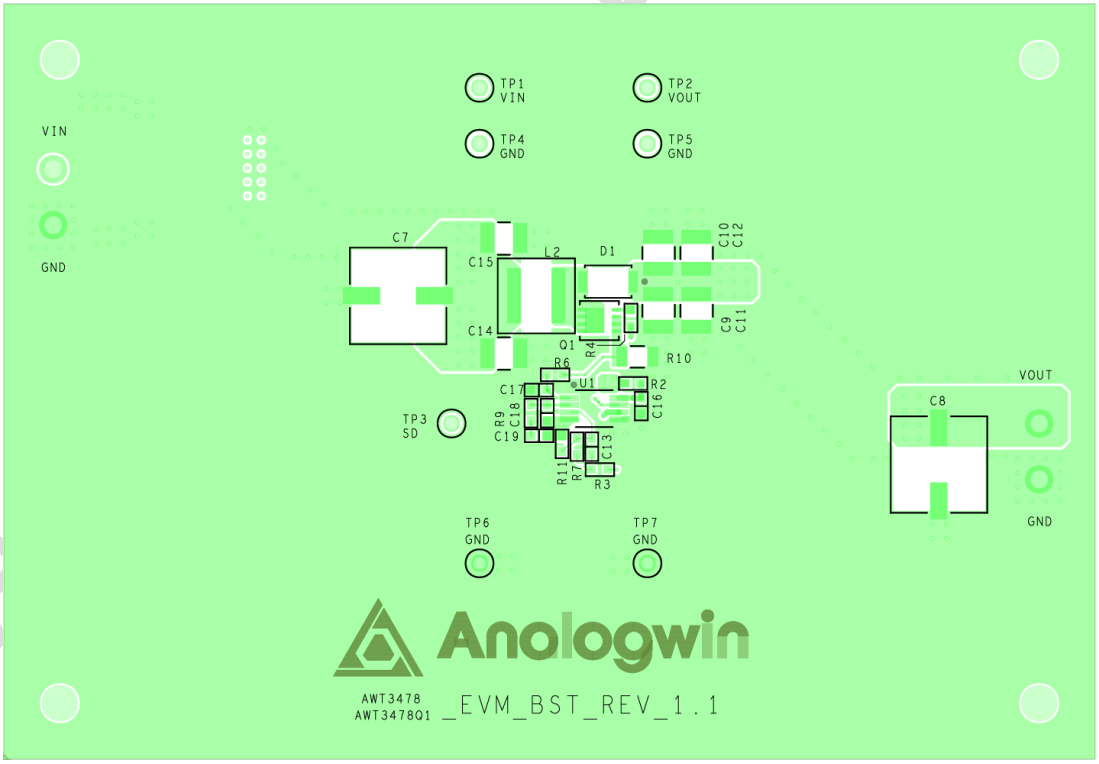


Fig. 25 Top Layer

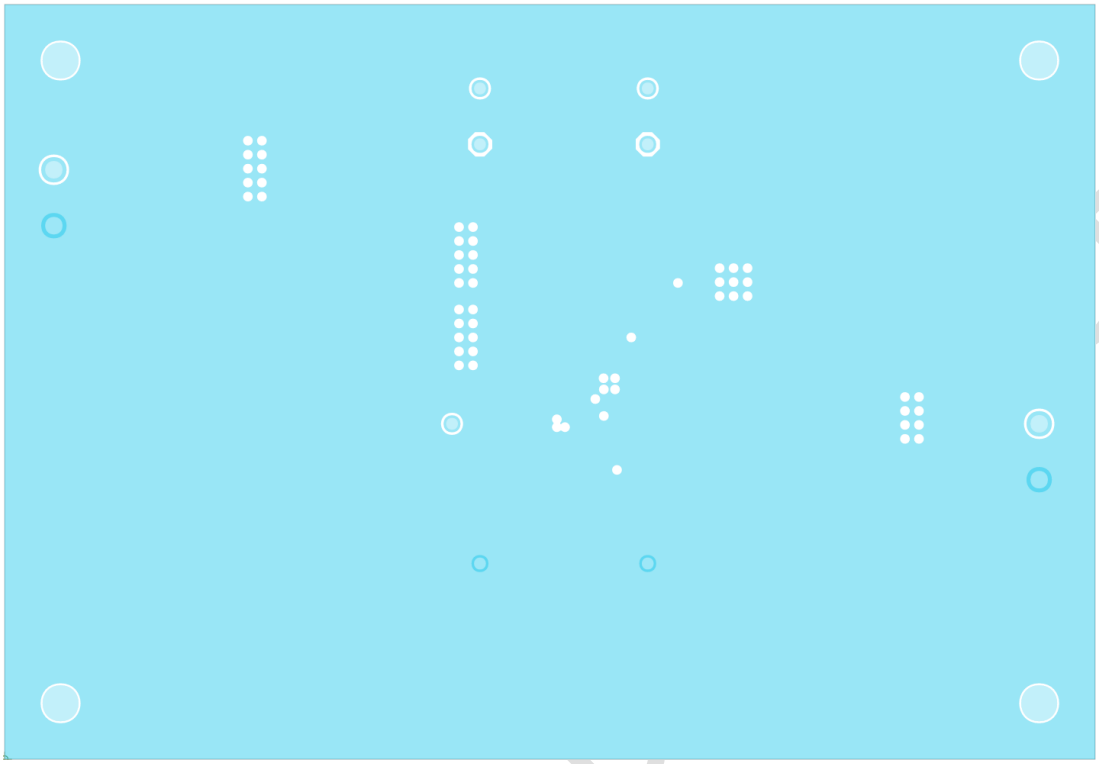


Fig.26 2nd Layer

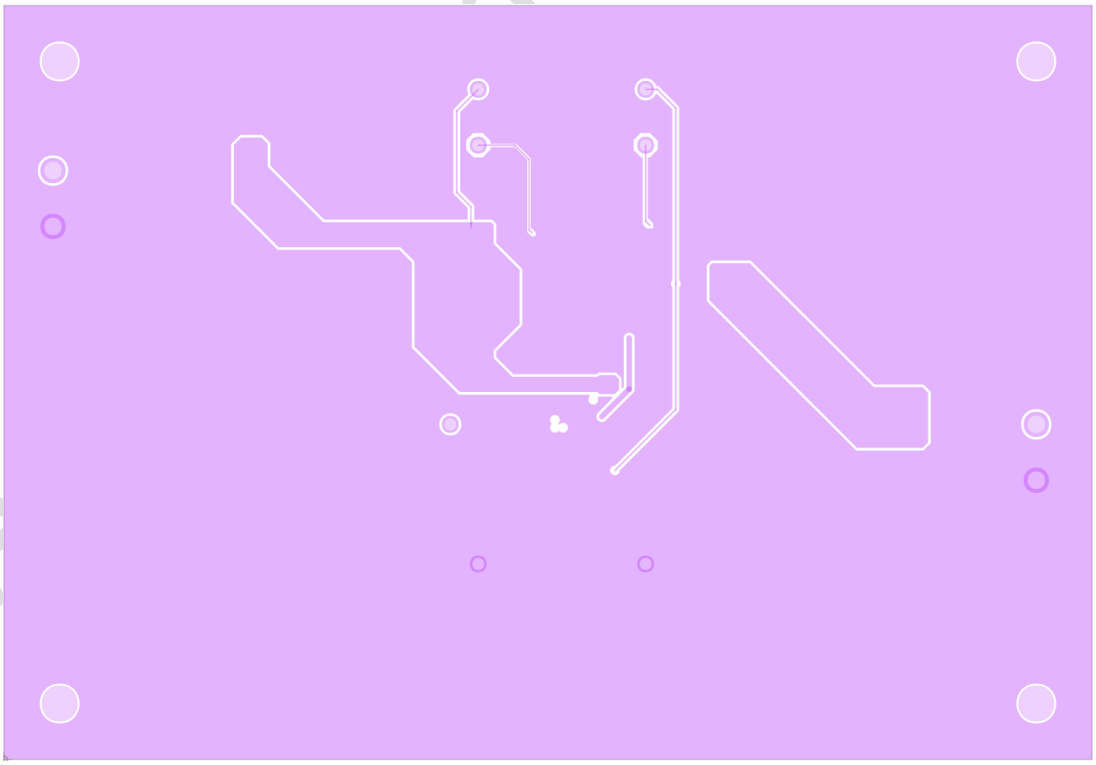


Fig.27 3rd Layer

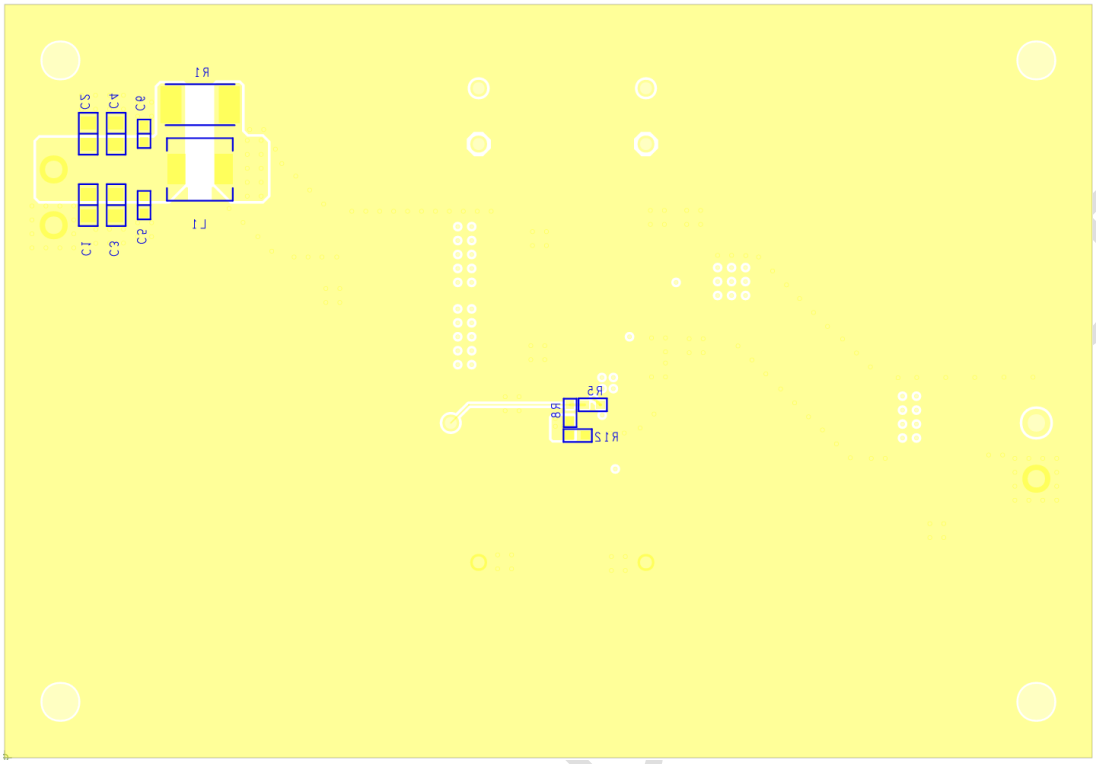


Fig.28 Bottom Layer

PACKAGE INFORMATION

Package Top marking

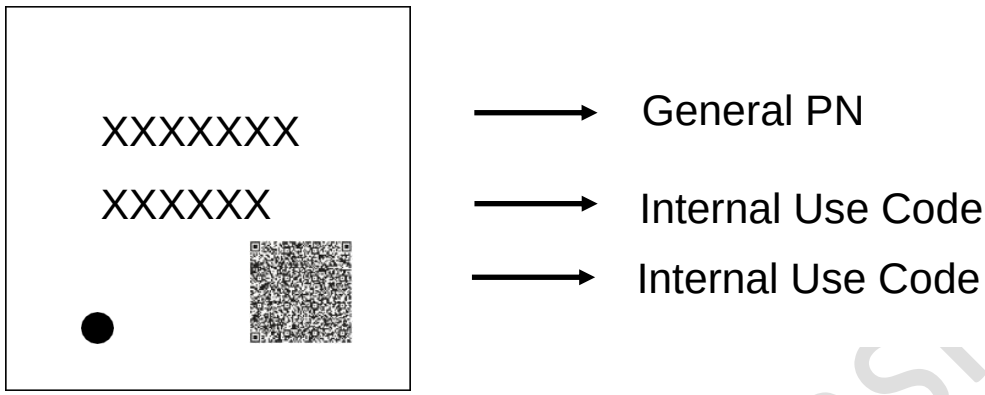


Fig.29 MSOP8L Package Top Marking

Tape and Reel Box Information

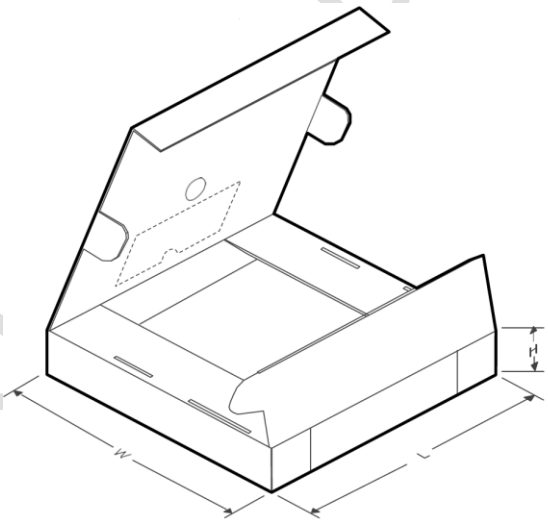


Fig.30 Tape and Reel Box Information

DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ	LENG (mm)	WIDTH (mm)	HEIGHT (mm)
AWT3478EARQ1	MSOP8L	EA	8	5000	336.0	336.0	48.0

Tape and Reel Information

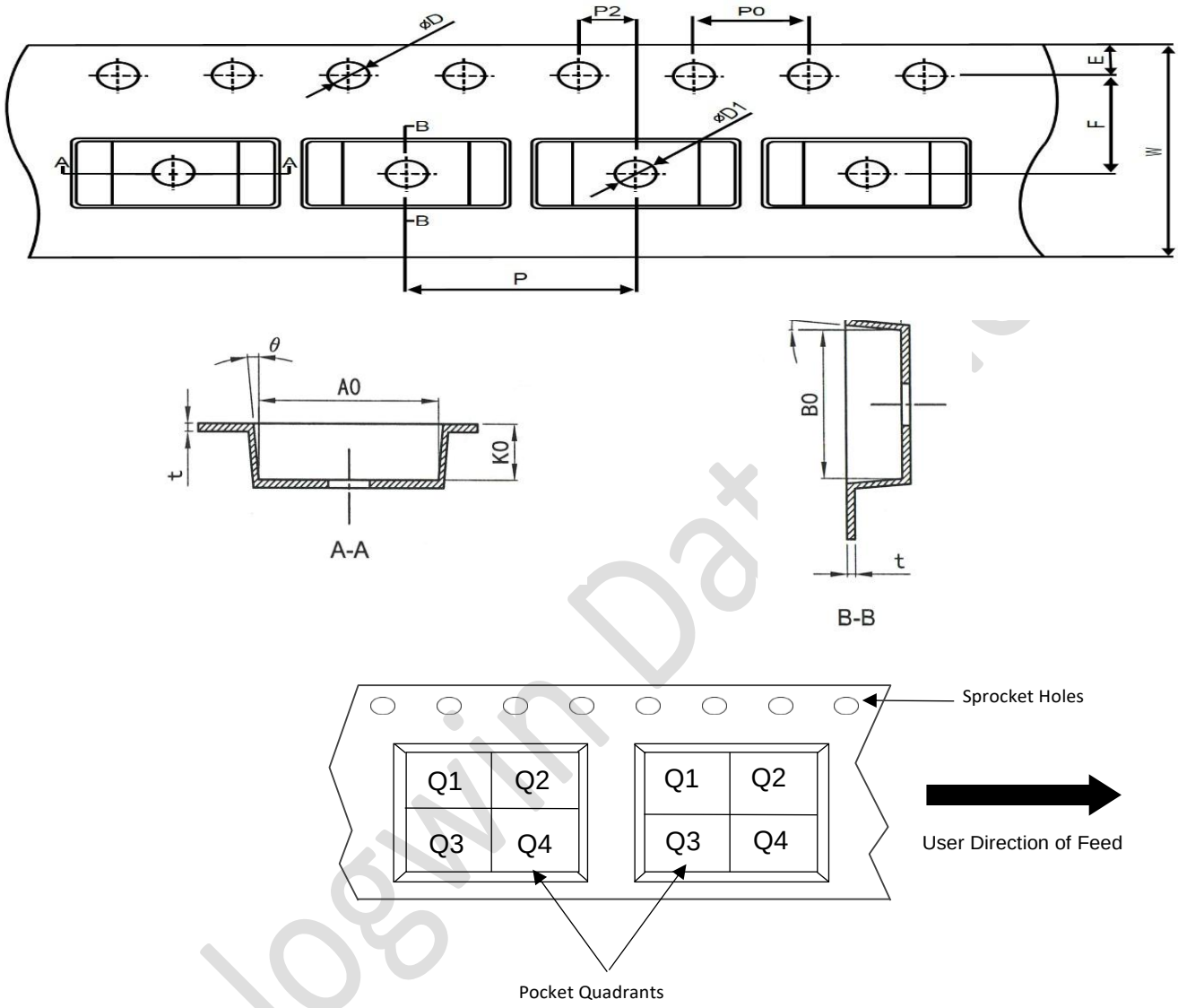


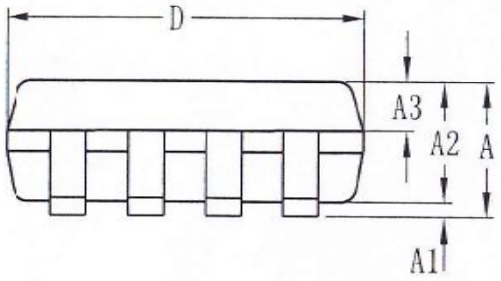
Fig.31 Tape and Reel Information

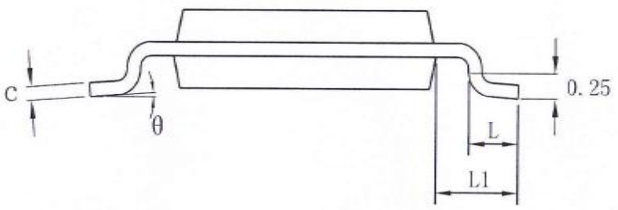
DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant	Quantity
AWT3478EARQ1	MSOP8	1.55	12.40	5.40	3.40	1.40	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

Package Outlines





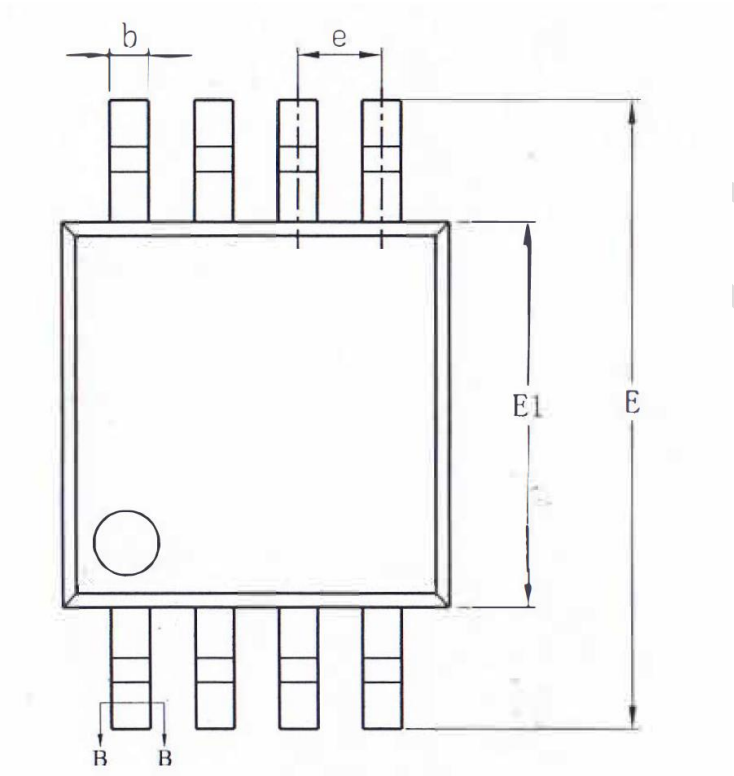


Fig.32 MSOP8L PKG POD

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.3	0.35	0.40
b	0.28	-	0.36
c	0.15	-	0.19
D	2.90	3.00	3.10
e	0.65BSC		
L1	0.95REF		
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
L	0.40	-	0.70
θ	0	-	8°

ORDERING INFORMATION

Order Part No.	Package	QTY
AWT3478EARQ1	MSOP8L, Pb-Free	5000/Reel

REVISION HISTORY

DATE	REVISION	NOTES
March. 2025	1.0	Initial release